CLAIMS

1. A digital frequency synthesizer comprising:

a first clock signal source for outputting a first clock signal;

a delay line including:

a delay line input coupled to the first clock signal source; and

a plurality of delay line output taps;

a plurality of multiplexers each of which include:

a plurality of multiplexer inputs coupled to the plurality of delay line output taps;

one or more multiplexer address inputs; and

a multiplexer output;

a common output coupled to the multiplexer outputs of the plurality of multiplexers;

a controller including:

a plurality of control signal outputs coupled to the one or more multiplexer address inputs of the plurality of multiplexers.

2. The digital frequency synthesizer according to claim 1 wherein:

each of the plurality of multiplexers comprise:

a windower for establishing a predetermined window of time during which each of the plurality of inputs of each multiplexer is coupled to the output of each multiplexer.

3. A digital frequency synthesizer comprising:

one or more delay lines including a plurality of output taps;

one or more clock signal sources coupled to the one or more delay lines;

one or more multiplexers including:

a plurality of signal inputs coupled to the plurality of output taps;

a plurality of address inputs; and

a common output;

a controller including a plurality of control signal outputs coupled to the plurality of address inputs, for causing the one or more multiplexers to couple a plurality of output taps to the common output during each of a plurality of periods of a clock signal generated by at least one of the one or more clock signal sources.

4. A digital frequency synthesizer comprising:

a common output;

a plurality of clock signal sources;

a plurality of delay lines each of which include;

a delay line input coupled to one of the plurality of clock signal sources;

a plurality of delay line taps;

a plurality of multiplexers each of which include:

a plurality of multiplexer inputs coupled to the delay line taps of one of the plurality of delay lines;

one or more multiplexer address inputs; and

a multiplexer output coupled to the common output.

5. The digital frequency synthesizer according to claim 4 further comprising:

a controller coupled to the one or more address inputs of the plurality of multiplexers.

6. A digital frequency synthesizer comprising:

a clock signal source for outputting a clock signal at a first frequency;

a delay line including:

a delay line input coupled to the clock signal source; and

a plurality of delay line output taps each of which is separated from the delay line input by a predetermined delay;

a common output;

a means for selectively coupling two or more output taps to the common output during a plurality of periods of the clock signal;

whereby a signal at a second frequency that exceeds the first frequency is output at the common output.

7. The digital frequency synthesizer according to claim 6 wherein

the plurality of delay line output taps are spaced by about a fraction of a period of the clock signal, wherein a denominator of the fraction is indivisible by a numerator of the fraction; and

the delay line is characterized by a propagation delay length of about the numerator of the fraction times the period of the clock signal.

8. A wireless communication device comprising:

a mixer including:

a first input for receiving a first signal that includes coded information;

a second input for receiving a locally generated signal for mixing with the first signal;

a digital frequency synthesizer including:

one or more delay lines including a plurality of output taps;

one or more clock signal sources coupled to the one or more delay lines;

one or more multiplexers including:

a plurality of signal inputs coupled to the plurality of output taps;

a plurality of address inputs; and

a common output coupled to the second input of the mixer; and

a controller including a plurality of control signal outputs coupled to the plurality of address inputs, for causing the one or more multiplexers to couple a plurality of output taps to the common output during a plurality of periods of a clock signal generated by at least one of the one or more clock signal sources.

9. A digital frequency synthesizer comprising:

a clock signal source for outputting a clock signal that is characterized by a clock signal period;

a first delay line including:

a first delay line input coupled to the clock signal source; and

a plurality of first delay line output taps;

a plurality of transmission gates each of which include:

a first signal terminal coupled to one of the plurality of first delay line output taps;

a second signal terminal coupled to a common output; and

a gate control terminal;

a plurality of decoders each of which includes:

one or more decoder address inputs; and

a plurality of decoder outputs;

a plurality of gate signal delay lines each of which is characterized by one of a plurality of delay durations and includes:

an input that is coupled a decoder output of each of the plurality of decoders;

an output coupled to the gate control terminal of one of the plurality transmission gates.

a controller including:

a set of control signal outputs coupled to the one or more decoder address inputs of the plurality of decoders.

10. The digital frequency synthesizer according to claim 9 wherein:

a delay associated with each gate signal delay line is commensurate with a delay that characterizes a tap of the first delay line that is coupled to a transmission gate to which the gate signal delay line is coupled.

11. The digital frequency synthesizer according to claim 9 wherein:

the delay line is characterized by a propagation delay length of about an integer multiple of the clock signal period.

12. The digital frequency synthesizer according to claim 9 wherein:

the plurality of first delay line output taps are spaced by about a fraction of the clock signal period, wherein a denominator of the fraction is indivisible by a numerator of the fraction; and

the first delay line is characterized by a propagation delay length of about the numerator of the fraction times the clock signal period.

13. The digital frequency synthesizer according to claim 9 wherein:

the first delay line further comprises:

a delay control input; and

the digital frequency synthesizer further comprises:

a phase detector including:

a first phase detector input coupled to the first delay line;

a second phase detector input coupled to the clock signal source;

a phase detector output;

a low pass filter including:

an low pass filter input coupled to the phase detector output; and

a low pass filter output coupled to the delay control input.

14. The digital frequency synthesizer according to claim 9 wherein the controller comprises:

a first adder including:

a first summand input for receiving a first control number;

a second summand input;

a first adder output coupled to the second summand input;

an overflow output; and

a first clock input coupled to the clock signal source;

a second adder including:

a second clock input coupled to the overflow output of the first adder;

a third summand input for receiving a second control number;

a fourth summand input;

a second adder output coupled to the fourth summand input

wherein the second adder output serves as a subset of the set of control signal outputs of the controller.

15. The digital frequency synthesizer according to claim 14 wherein the controller further comprises:

an overflow signal duration reducer coupled between the overflow output of the first adder and the second clock input.

16. The digital frequency synthesizer according to claim 14 wherein the controller further comprises:

one or more address modifiers, each of which is interposed between the second adder output and the one or more decoder address inputs of one of the plurality of decoders.

17. The digital frequency synthesizer according to claim 16 wherein the one or more address modifiers each comprise:

an address modifier adder for adding approximately an integer multiple of a ratio of a period of a signal to be synthesized and a period of the clock signal to an address output at the second adder output.

18. The digital frequency synthesizer according to claim 17 wherein the one or more address modifiers each comprise:

a selective delayer for determining if an incremented address output by the address modifier adder exceeds a predetermined maximum address and if so delaying the address in reaching the one or more address inputs of one of the plurality of decoders by one period of the reference clock.

19. A method of digitally synthesizing a signal, the method comprising the steps of:

generating a clock signal that includes a plurality of successive clock signal periods;

coupling the clock signal to a delay line that includes:

an input end;

a plurality of taps including:

a zeroth tap that is located closest to the input end; and

a last tap that is furthest from the input end; and

during at least one clock signal period, selecting and coupling two or more of the plurality of taps to an output.

20. The method according to claim 19 further comprising the steps of:

reducing a pulse width of the clock signal prior to coupling the clock signal to the delay line.

21. The method according to claim 19 wherein the step of selecting and coupling two or more of the plurality of taps to the output includes the steps of:

during each kth clock signal period selecting a plurality of taps that are spaced from each other by delays that when divided by a period of the clock signal yield remainders that are about equal to integer multiples of a generated signal period.

22. The method according to claim 21 wherein:

a last selected tap selected during each kth clock signal period is spaced from the zeroth tap by a first propagation delay that when divided by the clock signal period yields a first remainder that when subtracted from the clock signal period yields a difference that is less than the generated signal period,

selecting during a successive (k+1)th clock signal period a second selected tap that is spaced from the zeroth tap by second propagation delay that when divided by the clock signal period yields a second remainder that when added to the difference yields a sum that is equal to the generated signal period.

23. The method according to claim 19 wherein the step of coupling one or more of the plurality of taps to the output includes the steps of:

during each kth clock signal period coupling to the output a plurality of taps that are spaced from each by about a generated signal period.

24. The method according to claim 23:

the plurality of taps selected during each kth clock signal period includes:

a first selected tap that is positioned closest, among the plurality of taps, to the zeroth tap; and

a last selected tap that is positioned furthest, among the plurality of taps, from the zeroth tap; and

wherein a first propagation delay time between the zeroth tap and the last selected tap, during each kth clock signal period, when subtracted from the clock signal period yields a difference that when added to a second propagation delay time between the zeroth tap and the first selected tap for each successive (k+1)th clock signal period is equal to about the generated signal period.